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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,949	02/27/2004	Wen-Ting Chu	67,200-1248	6699

7590 11/29/2005

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EXAMINER	
NGUYEN, NAM THANH	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,949	CHU ET AL.	
	Examiner	Art Unit	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *EAST search*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (US Pat. No. 5,706,227) in view of Lojek (US Pat. No. 6,822,285).

Figure 1 of Chang et al disclose an N-type well region (18) formed in a substrate (20), the N-type well region (18) having formed therein a P+ source (14), a P+ drain (16), and a channel region (12) extending between the P+ source (14) and the P+ drain (16); a first insulating layer (29) disposed over the well region (18); a floating gate (22) disposed over the first layer (29), wherein the floating gate (22) is positioned over a first portion of the channel region (a half of the right channel region 12) but not a second portion of the channel region (a half of the left channel region 12); a second insulating layer (28) disposed over the floating gate (22); a control gate (26) including a first portion (a half of the left portion of control gate 26) disposed over the first insulating layer (29), the first portion of the control gate (see above) being positioned over the second portion of the channel region (see above), the control gate (26) including a second portion (a half of the right portion of control gate 26) disposed over the second insulating layer(28), and Chang et al fail to teach the cell which is operable to be

programmed by a band-to-band hot electron (BBHE) technique and erased by a polysilicon-polysilicon tunneling technique.

Lojek teaches that the cell could be programmed by band to band technique (see the abstract) and erased by a polysilicon-polysilicon tunneling technique (see col. 2, lines 53-61) for the purpose of preventing a hot hole conditions and over erasing data is well known in the art. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang et al by using band to band technique for programming and a polysilicon-polysilicon tunneling technique for erasing to prevent over erasing data and hot hole situation as taught by Lojek.

Regarding claim 2, fig. 1 of Chang et al disclose the second insulating layer (28) has a top wall portion (the portion that would be considered as a thickness of interpoly dielectric 28, see col. 3, lines 36-37) disposed over the floating gate (22) and a sidewall portion (the left side of the floating gate 22) of immediately adjacent to the floating gate.

Regarding claim 3, fig. 1 of Chang et al disclose the first portion of the control gate (a half of the left portion of control gate 26) is positioned immediately adjacent to the sidewall portion (the left side of the floating gate 22) of the second insulating layer (28), wherein the second portion of the control gate is disposed over the top wall portion (see claim 2 above) of the second insulating layer to minimize capacitive coupling with the floating gate.

Regarding claim 4, the channel region is a P-channel (see summary of the invention of Chang et al).

Claims 11-14 are rejected as being directed to the method or/and steps derived from the apparatus described in claims 1-4 above (i.e., steps each having one to one correspondence to the corresponding elements of the apparatus).

Claims 5-10 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (US Pat. No. 5,706,227) in view of Tran et al (US 2004/0125653).

Regarding claim 5, Chang et al applied as above. The difference between Chang et al and claim 5 is that Chang et al fail to teach the tip portion of the floating gate producing a stronger electric field compare to the memory cell without the tip.

Tran et al disclose (see paragraph 0120) the tip portion of the floating gate producing a stronger electric field compare to the memory cell without the tip in order to erase data of memory cell faster. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang et al by using the tip portion of the floating gate generating a stronger electric field compare to the memory cell without the tip for a purpose to erase data of memory cell faster as taught by Tran et al.

Regarding claim 6, Tran et al disclose the cell is operable by applying dual high voltages (see paragraph 0026).

Regarding claim 7, Tran et al disclose the cell is operable by applying single high voltages (see paragraph 0026).

Regarding claim 8, fig. 1 of Chang et al disclose the P+ drain is coupled to a bit line of the cell. (It is noted that the drain must be coupled to the bit line as well known in the memory art).

Regarding claim 9, fig. 1 of Chang et al disclose the control gate is coupled to a word line of the cell. (It is noted that the control gate must be coupled to the bit line as well known in the memory art).

Claims 10 and 15-19 are rejected as being directed to the method or/and steps derived from the apparatus described in claims 5-9 above (i.e., steps each having one to one correspondence to the corresponding elements of the apparatus).

Conclusion

3. The following prior art, which is considered pertinent to applicant's disclosure although not relied upon, includes:

Lin et al (US pat. No. 6,363,012) or Kuo et al (US Pat. No. 5,130,769) disclose a split gate flash similar to that of the present application, but fail to disclose the claimed limitations as described above.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T. Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam T Nguyen
Examiner
Art Unit 2824

11/16/05
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VAN THU NGUYEN
PRIMARY EXAMINER